REPLACEMENT SHEET

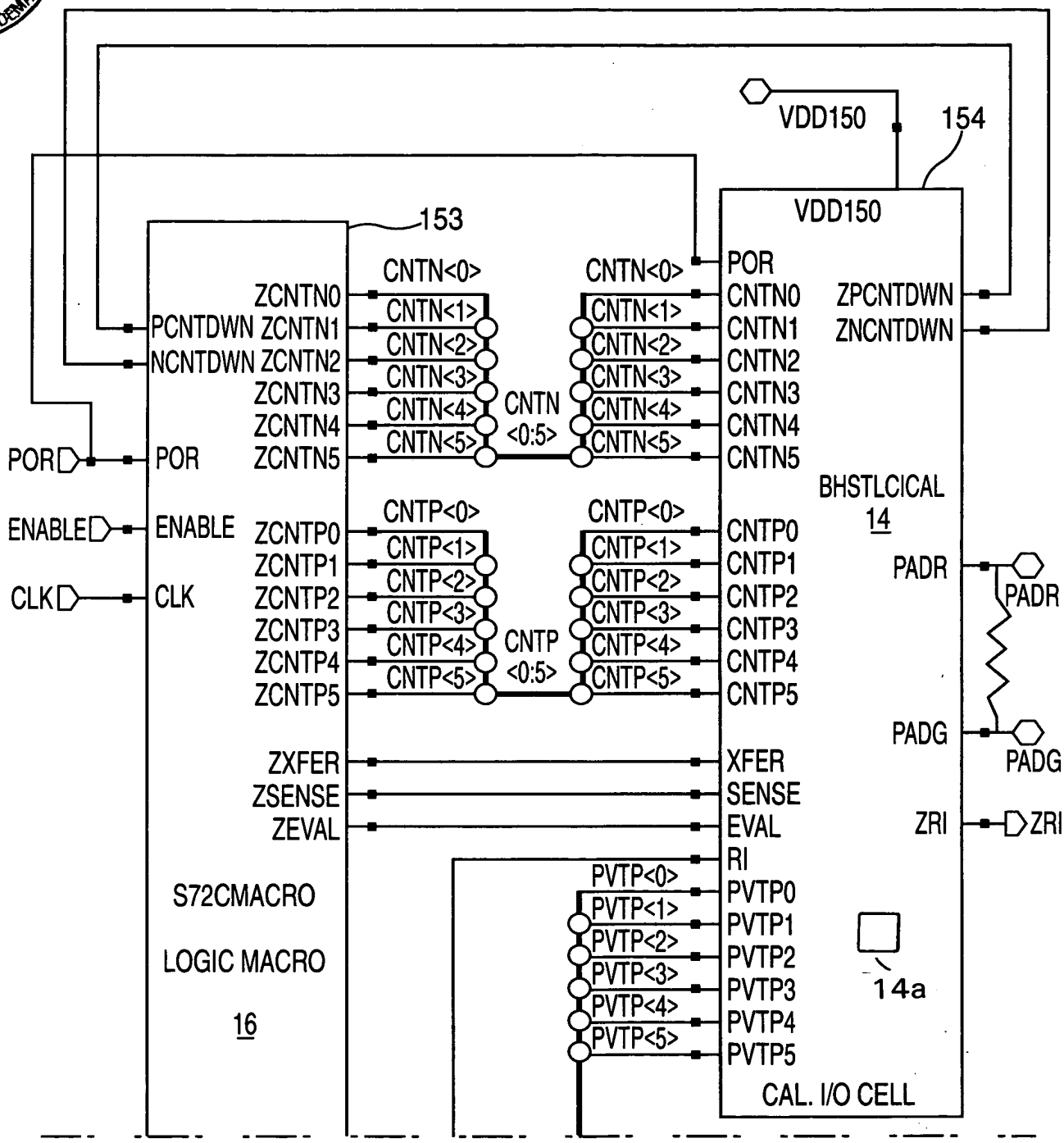


FIG. 2A

2-A
2-B

FIG. 2

REPLACEMENT SHEET

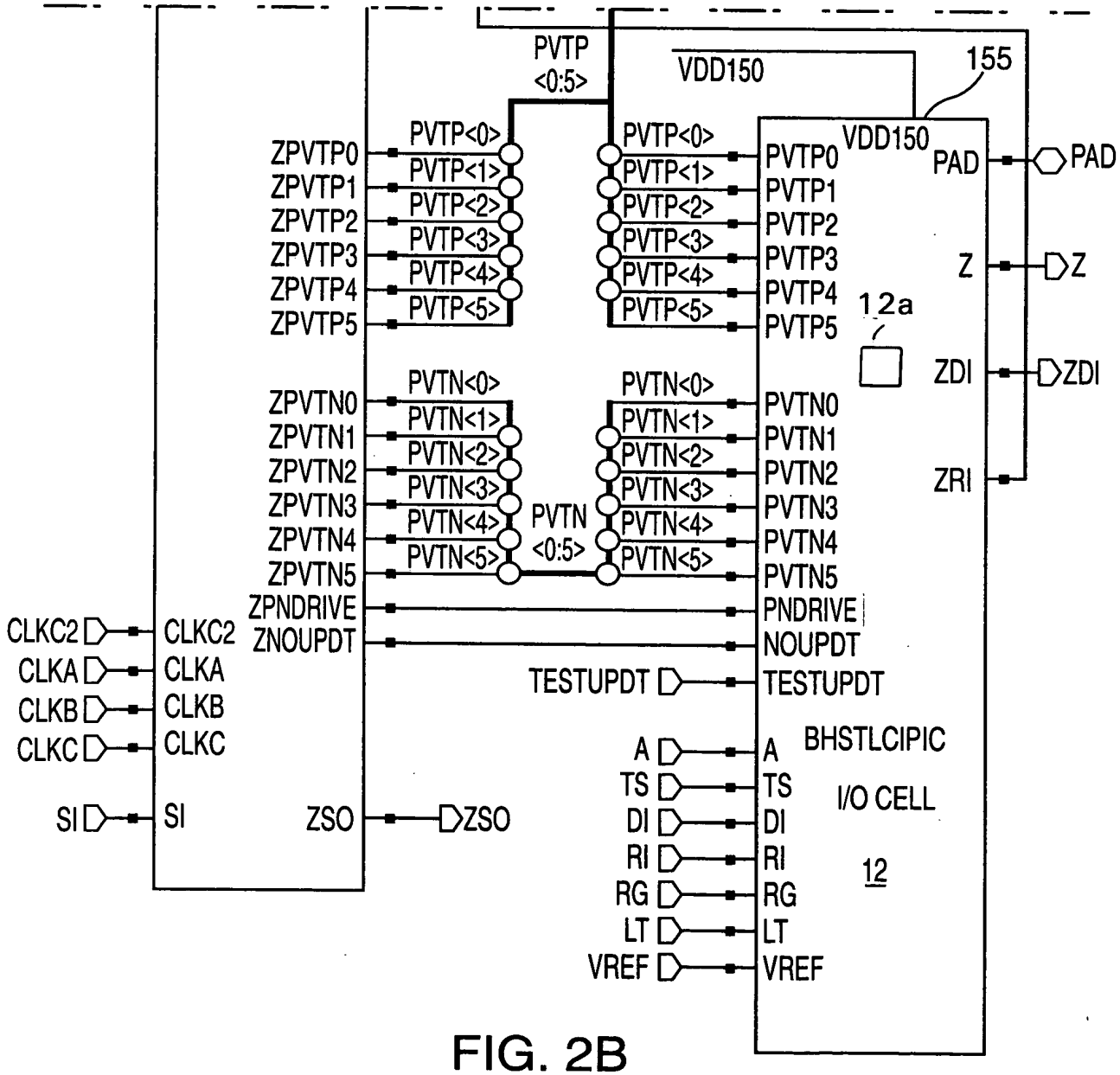
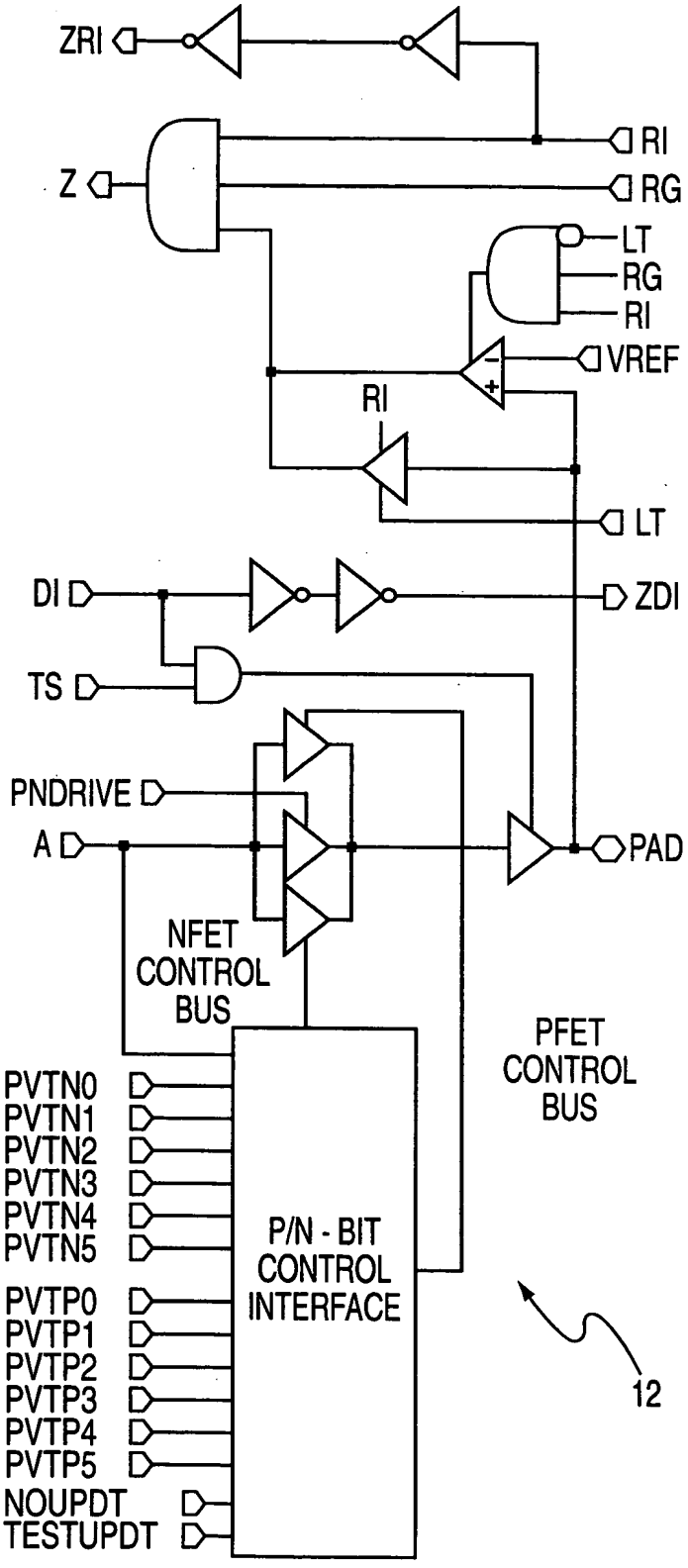


FIG. 2B

A	DRIVER DATA INPUT
TS	DRIVER TRI-STATE CONTROL
DI	DRIVER INHIBIT INPUT (DI IN)
LT	DC CURRENT GATE (I_{dd} TEST) INPUT
RI	RECEIVER INHIBIT INPUT (RI IN)
RG	RECEIVER GATE CONTROL
VREF	VOLTAGE REFERENCE INPUT
PAD	DRIVER OUTPUT/RECEIVER INPUT
ZDI	DRIVER INHIBIT OUTPUT (DI OUT)
ZRI	RECEIVER INHIBIT OUTPUT (RI OUT)
Z	RECEIVER OUTPUT
PVTN0	NFET PVT CONTROL BIT (LSB)
PVTN1	NFET PVT CONTROL BIT
PVTN2	NFET PVT CONTROL BIT
PVTN3	NFET PVT CONTROL BIT
PVTN4	NFET PVT CONTROL BIT
PVTN5	NFET PVT CONTROL BIT (MSB)
PVTP0	PFET PVT CONTROL BIT (LSB)
PVTP1	PFET PVT CONTROL BIT
PVTP2	PFET PVT CONTROL BIT
PVTP3	PFET PVT CONTROL BIT
PVTP4	PFET PVT CONTROL BIT
PVTP5	PFET PVT CONTROL BIT (MSB)
PNDRIVE	DEFAULT CONTROL BIT
NOUPDT	PREVENTS BIT UPDATE
TESTUPDT	UPDATES BITS



CONTROLLED I/O CELL

FIG. 3